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PATENT APPLICATION

INTEGRATION SCHEME USING SELF-PLANARIZED DIELECTRIC LAYER FOR SHALLOW TRENCH ISOLATION

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Status: Large Entity

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Application Information

Title Line One:: INTEGRATION SCHEME USING SELF-PLANARIZED

Title Line Two:: DIELECTRIC LAYER FOR SHALLOW TRENCH ISOLATION

Formal Drawings?::

Application Type::

Utility

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Secrecy Order in Patent Appl.?:: No

Prior Foreign Applications

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Foreign Application Two:: EP99402068.3 Filing Date:: EP99402068.3

Country:: Europe
Priority Claimed:: Yes